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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/586,433	06/02/2000	Ulrich Bortfeld	252/024	7379

25700 7590 09/27/2004

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/586,433	BORTFELD, ULRICH
	Examiner	Art Unit
	Dwin M Craig	2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-17 have been presented for reconsideration in view of Applicant's amended claim language and arguments.

Response to Arguments

2. Applicant's arguments submitted in the 23 June 2004 response have been fully considered. The Examiner's response is as follows.

2.1 Regarding the Applicants submission of a terminal disclaimer in response to the Judicially Created NON-Statutory Double Patenting rejections of Independent Claim 1.

The Examiner thanks the Applicant for submitting a terminal disclaimer and withdraws the earlier obvious type Judicially created NON-Statutory Double Patenting rejected of Independent Claim 1.

2.2 Regarding the Applicant's amendment to the specification in regards to the I Examiner's objection to the Specification for Improper Incorporation by Reference of Patent Application number 09/586,325.

The Examiner thanks the Applicant for inserting the correct serial numbering the specification and withdraws the objection to the same.

2.3 Regarding the Applicant's response to the 35 U.S.C. 102(b) rejections of Claims 1, 7, 11, 12 and 15.

Applicant argued;

> In Gupta, simulation of hardware and software is performed separately. Gupta does not teach a unified simulation that runs as a single process...

The Examiner has found Applicant's arguments to be persuasive and withdraws the earlier 35 U.S.C. 102(b) rejections of Claims 1, 7, 11, 12 and 15.

2.4 Regarding the Applicant's response to the 35 U.S.C. 102(b) rejections of Claims 1-17.

Applicant argued;

Ball does not tech a unified simulation that runs as a single process

The Examiner has found Applicant's arguments to be persuasive and withdraws the earlier 35 U.S.C. 102(b) rejections of Claims 1-15.

An updated search has revealed new art.

Claim Interpretation

3. The term/phrase "unified simulation" in Independent **Claims 1, 7, 11, 12 and 15** is used by the Applicant to mean "allowing a single simulation environment to simulate both hardware components (memory and processor) as well as a software component (the operating system environment" (see page 13 of Applicant's 23 June 2004 response and page 18 of the Specification), while the accepted meaning is "The simulation of Analog and mixed signals simulation. (See U.S. Patent 6,266,630 Col. 1 Lines 40-53)." For the purposes of Examination the Examiner will treat the phrase, "unified simulation" to mean the simulation of both hardware and software in a single process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Independent **Claims 1, 7, 11, 12 and 15** and dependent **Claim 2** are rejected under **35 U.S.C. 103(a)** as being unpatentable over **"Synthesis and Simulation of Digital Systems Containing Interacting Hardware and Software Components**, by Rajesh K. Gupta, Claudionor Nunes Coelho, Jr., and Giovanni De Micheli," hereafter reffered to as the *Gupta et al.* reference in view of **Rompacy et al. U.S. Patent 5,870,588**.

4.1 As regards independent **Claims 1, 7, 11, 12 and 15** the *Gupta et al.* refernece discloses, a unified simulation design/program product/method for simulating system design **(page 225)**, identifying a memory component and a processor component of a system design **(Figure 2 and pages 225-226)**, associating said software component with said programming model of said memory component within a simulation environment **(pages 228-**

230 section 4 Simulation of Hardware-Software Systems), executing said system design and said application program in said simulation environment **(Figure 7 page 230 and section 5 Conclusions).**

However, the *Gupta et al.* refernece does not expressly disclose a simulation of hardware and software in a *"unified simulation"* as defined by the Applicant and further having that *"unified simulation"* run as a single process.

In the system simulation art, the *Rompacy et al.* refernece discloses a *"unified simulation"* **(Figure 6** *Note the "uproc SW model" and the "uproc HW model"* **and Figure 9 Items 86 and 87 and 88, Col. 6 Lines 6-18, Col. 6 Lines 45-54),** and the *"merging"* of multiple process into a single process to simulate both hardware and software **(Col. 6 Lines 57-67, Col. 7 Lines 1-31** *(Note the phrase "merging the plurality of processes" on lines 27 & 28 which is functionally equavalent to having a single process)*.

It would have been obvious, to one of ordinary skill in the art, at the time the invnetion was made, to have combined the teachings of the *Gupta et al.* refernece with the teachings of the *Rompacy et al.* reference because, by providing a mechanism to simulate and synthesize all of the hardware and software components using a conventional development tools allows for a better, refined simulation of the complete system using one simulation tool as opposed to having to simulate and debug a hardware/software design using multiple development tools, this allows for savings of both time and money ***(see Rompacy et al. Col. 10 Lines 53-63)*.**

4.2 As regards dependent **Claim 2** the *Gupta et al.* refernece teaches generating cycle accurate information **(pages 227-228).**

5. **Claims 1-17 are rejected** under **35 U.S.C. 103(a)** as being unpatentable over **Ball U.S. Patent 5,615,357** in view of **Rompacy et al. U.S. Patent 5,870,588.**

5.1 As regards independent **Claims 1, 7, 11, 12 and 15** the *Ball* reference discloses, a unified simulation design/program product/method for simulating system design **(Figure 5A),** identifying a memory component and a processor component of a system design **(Figure 2, Col. 6 Lines 54-67),** associating said software component with said programming model of said memory component within a simulation environment **(Col. 6 Lines 36-51),** executing said system design and said application program in said simulation environment **(Col. 12 Lines 22-55).**

However, the *Ball* refernece does not expressly disclose a simulation of hardware and software in a *"unified simulation"* as defined by the Applicant and further having that *"unified simulation"* run as a single process.

In the system simulation art, the *Rompacy et al.* refernece discloses a *"unified simulation"* **(Figure 6** *Note the "uproc SW model" and the "uproc HW model"* **and Figure 9 Items 86 and 87 and 88, Col. 6 Lines 6-18, Col. 6 Lines 45-54),** and the *"merging"* of multiple process into a single process to simulate both hardware and software **(Col. 6 Lines 57-67, Col. 7 Lines 1-31** *(Note the phrase "merging the plurality of processes" on lines 27 & 28 which is functionally equavalent to having a single process).*

It would have been obvious, to one of ordinary skill in the art, at the time the invnetion was made, to have combined the teachings of the *Ball* reference with the teachings of the *Rompacy et al.* reference because, by providing a mechanism to simulate and synthesize all

of the hardware and software components using a conventional development tools allows for a better, refined simulation of the complete system using one simulation tool as opposed to having to simulate and debug a hardware/software design using multiple development tools, this allows for savings of both time and money ***(see Rompacy et al. Col. 10 Lines 53-63)***.

5.2 As regards dependent **Claims 2, 13 and 16** the *Ball* refernece discloses cycle accurate information **(Figures 3B, 5A Item 60)**.

5.3 As regards dependent **Claims 3, 8 and 9** the *Ball* reference discloses high level functions calls and software *links* between the different executing modules **(Col. 3 Lines 26-67, Col. 4 Lines 1-34, Col. 6 Lines 35-67)**.

5.4 As regards dependent **Claims 4-6** the *Ball* reference discloses **(Col. 9 Lines 56-65, Col. 10, 11, 12, 13, Figures 3A, 3B, 4A, 4B, 5A, 6A, 6B, 6D)**.

5.5 As regards dependent **Claim 10** the *Ball* reference discloses a clock **(Figure 3B CYCLES)**.

5.6 As regards dependent **Claim 14** the *Ball* reference discloses sets of instructions **(Figures 3B, 4A, 4B)**.

5.7 As regards dependent **Claim 17** the *Ball* reference discloses instructions associated with the memory model **(Figure 4A Item 26: LOAD MEM, Col. 10 Lines 54-64)**.

Conclusion

6. **Claims 1-17** have been presented for reconsideration in view of Applicant's amended claim language. **Claims 1-17** are rejected.

6.1 Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC